ST. ALOYSIUS COLLEGE (AUTONOMOUS), JABALPUR

PART A: Introduction

Program: Certificate	Class: B.Sc.	Year: I Year (sem 1)	Session: 2022-23
Subject: Computer Science			
I.	Course Code	S I-COSC 1T	
2.	Course Title	Computer System Architecture (Paper 1)	
3.	Course Type (Elective/Generic Elective)	Elective Course	
4.	Pre-Requisite (if any)	To study this course, a student must have had the subject Physics/ Math in 12th class.	
5.	Course Outcomes(CO)	On completion of this course, learners will be able to: CO1. Understand the basic structure, operation and characteristics of digital computer. CO2. Be able to design simple combinational digital circuits based on given parameters. CO3. Familiarity with working of arithmetic and logic unit as well as the concept of pipelining. CO4. Know about hierarchical memory system including cache memories and virtual memory. CO5. Understand concept and advantages of parallel ism, threading, multi-processors and multi-core processors. Know the contributions of Indians in the field of computer architecture and related technologies.	
6.	Credit Value	Theory 3 Credits	
7.	Total Marks	Max. Marks : 100	Min. Passing Marks: 35

PART B: Content of the Course		
Module	Topics	No. of Lectures
I	Fundamentals of Digital Electronics: Number System, Conversions, Binary Arithmetic, Complements, Fixed-Point Representation, Floating-Point Representation, Binary and other Codes, Error Detection Codes.	10
II	Logic Gates, Boolean Algebra, Map Simplification, K-Map, Combinational Circuits, Sequential Circuits, Simple Combinational circuit design problems.	10
III	Combinational Circuits- Adder, Subtractor, Multiplexer, De-multiplexer, Decoders, Encoders, Sequential Circuits - Flip - Flops, SR, D, T, JK,, Registers, Types of Registers, Counters, Types of Counters.	10
IV	Instructions, Instructions Formats, RISC, CISC, DMA Data Transfer, Auxiliary Memory, Cache Memory, Associative Memory, Virtual Memory, Flynn's classification - Introduction to SISD, SIMD, MISD, MIMD, Parallelism, Multicore processors.	10
Keywords/Tags: Digital Electronics, Logic Gates, Circuits, Instruction formats, Parallelism, Memory hierarchy, Multicore, Multi-threading, SISD, SIMD, MISD, MIMD.		
PART C: Learning Resources		
Textbooks, Reference Books, Other Resources		
Suggested Readings: • M. Morris Mano, "Computer System Architecture", PHI. • Heuring Jordan , "Computer System Design & Architecture" (A.W.L.) • William Stalling, "Computer Organization & Architecture", Pearson Education Asia. • V. Carl Hamacher , "Computer Organizat ion", TMH • Tannenbaum, "Structured Computer Organization ", PHI.		

PART D: Assessment and Evaluation			
Internal Assessment : Continuous Comprehensive Evaluation (CCE) : 40 **Marks** Three test will be taken of which best of two marks will be considered		**External Assessment**: University Exam (UE) : 60 **Marks** Time : **02.00 Hours**	
Objective type Text I	20 Marks	Section (A) : Very short questions (1 from each unit)	1 x 5 = 5 Marks
Class Test II (Subjective)	20 Marks	Section (B) : 5 Short Questions (200 Words Each)	4 x 5 = 20 Marks
Class Test III (**Subjective**)	20 Marks		
		Section (C): 5 Long Questions (500	7 x 5 = 35

		Words Each)	Marks
Total	**40 Marks**	Total	**60 Marks**

PART D: Content of the Course		
No. of Lab. Practical s (in hours per week): 2 Hrs. per week		
Total No. of Labs:		
	Suggestive list of Practical	No. of Labs.
	1. To study basic gates (AND, OR, NOT) and verify their truth tables. 2. To study and verify NAND as Universal gate using IC 7400. 3. To realize basic gate AND from Universal gate NAND. 4. To realize basic gate OR from Universal gate NAND. 5. To realize basic gate N OT from Universal gate NAND. 6. To study and verify NOR as Universal gate 7. To realize basic gate AND from Universal gate NOR. 8. To realize basic gate OR from Universal gate NOR. 9. To realize basic gate NOT from Universal gate NOR. 10. To study Half Adder using basic gates and verify its truth table. 11. To study Full Adder using basic gates and verify its truth table. 12. To design and construct RS flip Flop using gates and verifies the truth table. 13. To design and construct JK Flip Elop using gates and verifies the truth table. 14. To verify De-Morgan's First Law Theorem. 15. To verify De-Morgan's Second Law Theorem.	
	Keywords/Tags: Digital Electronics, Logic Gates, AN D, OR, NOT, IC7486, IC 7400, NAND, NOR, IC 7483, Circuits, Flip Flop, De-Morgan's	

PART D: Assessment and Evaluation			
Internal Assessment : Continuous Comprehensive Evaluation (CCE) : 40 **Marks**		**External Assessment**: University Exam (UE) : **60 Marks** Time : **02.00 Hours**	
Internal Assessment	**Marks**	**External Assessment**	**Marks**
Lab Attendance	10 Marks	Practical record file	25 Marks
		Viva voce practical	10 Marks
Internal Viva	10 Marks	Execution	05 Marks
Practical File	20 Marks	Answer script	20 Marks
Total	**40 Marks**	**Total**	**60 Marks**

ST. ALOYSIUS COLLEGE (AUTONOMOUS), JABALPUR

PART A: Introduction

PROGRAM: Certificate | CLASS: B.Sc. | SEMESTER: I | SESSION: 2022-23

Subject: Computer Science

1.	Course Code	S1 - COSC 1T
2.	Course Title	Computer System Architecture (Paper I)
3.	Course Type	Major/Minor
4.	Pre-Requisite (if any)	To study this course, a student must have had the subject Physics/ Math in 12th class.
5.	Course Learning Outcomes(CO)	On completion of this course, learners will be able to: CO1. Understand the basic structure, operation and characteristics of digital computer. CO2. Be able to design simple combinational digital circuits based on given parameters. CO3. Familiarity with working of arithmetic and logic unit as well as the concept of pipelining. CO4. Know about hierarchical memory system including cache memories and virtual memory. CO5. Understand concept and advantages of parallel ism, threading, multi-processors and multi-core processors. Know the contributions of Indians in the field of computer architecture and related technologies.
6.	Credit Value	Theory 4 Credits
7.	Total Marks	Max. Marks : 100 | Min. Passing Marks: 35

PART B: Content of the Course

No. of Lectures (in hours per week): 2 Hrs. per week

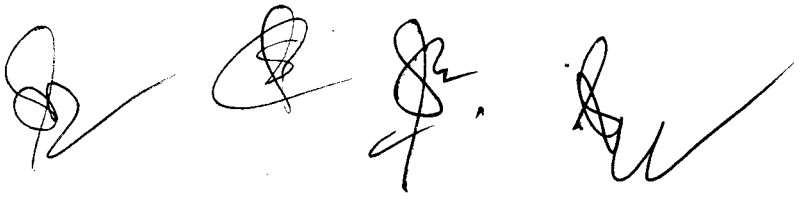
Total No. of Lectures: 60 Hrs.

Module	Topics	No. of Lectures
I	Fundamentals of Digital Electronics: Number System-Binary, Decimal, Octal, Hexa-Decimal, Conversions, Binary Arithmetic-Addition, Subtraction, Multiplication, Division, Underflow, Overflow, Sign Magnitude, Complements-1's and 2's, Fixed-Point Representation, Floating-Point Representation.	10
II	Boolean Algebra, Reducing Boolean Expression, Logic Gates-AND, OR, NOT, Universal Gates-NAND, NOR, Analog and Digital Signals, Clock Waveform Timing, Map Simplification, K-Map- Two, Three and Four variables.	10

III	Combinational Circuits- Adder, Subtractor, Multiplexer, De-multiplexer, Decoders, Encoders, Binary Codes – Gray Codes, ASCII code, BCD code, EBCDIC, Error Detection Code and Correction Code, Hamming Code.	10
IV	Sequential Circuits - Flip - Flops, SR, D, T, JK, Master-Slave, Registers, Shift Registers- SISO, SIPO, PISO, PIPO, Counters, Instruction, Instruction Format, Instruction Codes, instructions Cycles, Addressing Modes.	10
V	Handshaking, Concepts of RISC, CISC, DMA Data Transfer, Auxiliary Memory, Cache Memory, Associative Memory, Virtual Memory, Flynn's classification - Introduction to SISD, SIMD, MISD, MIMD, Parallelism, Multicore processors.	10
Keywords/Tags: Digital Electronics, Logic Gates, Circuits, Instruction formats, Parallelism, Memory hierarchy, Multicore, Multi-threading, SISD, SIMD, MISD, MIMD.		

PART D: Assessment and Evaluation			
Internal Assessment : Continuous Comprehensive Evaluation (CCE) : 40 **Marks** Three test will be taken of which best of two marks will be considered		**External Assessment**: University Exam (UE) : 60 **Marks** Time : **02.00 Hours**	
Objective type Text I	20 Marks	Section (A) : Very short questions (1 from each unit)	1 x 5 = 5 Marks
Class Test II (Subjective)	20 Marks	Section (B) : 5 Short Questions (200 Words Each)	4 x 5 = 20 Marks
Class Test III **(Subjective)**	20 Marks	Section (C): 5 Long Questions (500 Words Each)	7 x 5 = 35 Marks
Total	**40 Marks**	Total	**60 Marks**
Any remarks/suggestions: **Focus of the course/teaching should be on developing ability of the student in analyzing a problem, building the logic and efficient code for the problem.**			

PART D: Content of the Course		
No. of Lab. Practical s (in hours per week): 2 Hrs. per week		
Total No. of Labs: 15Labs (30 HRS)		
	Suggestive list of Practical	No. of Labs.
	1. To study basic gates (AND, OR, NOT) and verify their truth tables. 2. To study and verify NAND as Universal gate using IC 7400. 3. To realize basic gate AND from Universal gate NAND. 4. To realize basic gate OR from Universal gate NAND. 5. To realize basic gate N OT from Universal gate NAND. 6. To study and verify NOR as Universal gate 7. To realize basic gate AND from Universal gate NOR. 8. To realize basic gate OR from Universal gate NOR. 9. To realize basic gate NOT from Universal gate NOR. 10. To study Half Adder using basic gates and verify its truth table. 11. To study Full Adder using basic gates and verify its truth table. 12. To design and construct RS flip Flop using gates and verifies the truth table. 13. To design and construct JK Flip Flop using gates and verifies the truth table. 14. To verify De-Morgan's First Law Theorem. 15. To verify De-Morgan's Second Law Theorem. 16. To study basic gates (AND, OR, NOT) and verify their truth tables. 17. To study and verify NAND as Universal gate using IC 7400. 18. To realize basic gate AND from Universal gate NAND. 19. To realize basic gate OR from Universal gate NAND. 20. To realize basic gate N OT from Universal gate NAND. 21. To study and verify NOR as Universal gate 22. To realize basic gate AND from Universal gate NOR. 23. To realize basic gate OR from Universal gate NOR. 24. To realize basic gate NOT from Universal gate NOR. 25. To study Half Adder using basic gates and verify its truth table. 26. To study Full Adder using basic gates and verify its truth table. 27. To design and construct RS flip Flop using gates and verifies the truth table. 28. To design and construct JK Flip Flop using gates and verifies the truth table. 29. To verify De-Morgan's First Law Theorem. 30. To verify De-Morgan's Second Law Theorem.	15
	Keywords/Tags: Digital Electronics, Logic Gates, AN D, OR, NOT, IC7486, IC 7400, NAND, NOR, IC 7483, Circuits, Flip Flop, De-Morgan's Theorem.	



PART D: Assessment and Evaluation			
Internal Assessment : Continuous Comprehensive Evaluation (CCE) : 40 **Marks**		**External Assessment**: University Exam (UE) : **60 Marks** Time : **02.00 Hours**	
Internal Assessment	**Marks**	**External Assessment**	**Marks**
Lab Attendance	10 Marks	Practical record file	25 Marks
		Viva voce practical	10 Marks
Internal Viva	10 Marks	Execution	05 Marks
Practical File	20 Marks	Answer script	20 Marks
Total	**40 Marks**	**Total**	**60 Marks**